



IPW

PATENT
Docket No. INTEL/17225

IN THE UNITED STATES PATENT
AND TRADEMARK OFFICE

Applicants:

TIAN et al.

U.S. Serial No.: 10/677,414

For: "Methods and Apparatus for
Reducing Memory Latency
in a Software Application"

Filed: October 2, 2003

Assignee: Intel Corporation

Group Art Unit: 2121

Examiner: Not Yet Assigned

) I hereby certify that this paper and the
documents referred to as enclosed
therewith are being deposited with the
United States Postal Service as first
class mail, postage prepaid, in an
envelope addressed to Commissioner
for Patents, P.O. Box 1450,
Alexandria, Virginia 22313-1450 on
this date:
)
October 14, 2004


Mark C. Zimmerman
Attorney for Applicant(s)
Registration No. 44,006

STATUS LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Kindly advise when an Office action can be expected in the above-referenced
matter.

Respectfully submitted,

GROSSMAN & FLIGHT, LLC
20 North Wacker Drive
Suite 4220
Chicago, Illinois 60606
(312) 580-1020

October 14, 2004

By:



Mark C. Zimmerman
Registration No.: 44,006

Attorneys for Intel Corporation